

IN THE DRAWINGS

Please find enclosed a copy of Fig. 8, as originally filed, with proposed amendments indicated in red thereon for the Examiner's approval.

The diagram illustrates a PLL system with two feedback paths. Path 20 includes a Digital Signal Gen. (10) connected to a Multiplier (21). The output of 21 is connected to an Adder (23). The output of 23 is labeled 'TO AMPLIFIER'. A feedback loop from the output of 23 goes through a Frequency Divider (24) and back to the input of 21. Path 30a starts with a Local Oscillator (70) connected to a Frequency Divider (31). The output of 31 is connected to a Frequency Mixer (32). The output of 32 is connected to another Frequency Mixer (34). The output of 34 is connected to a BPF (33). The output of 33 is connected to a Frequency Divider (24) and back to the input of 21. The output of 21 is also connected to the input of 32.

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